82S140-F,N • 82S141-F,N

## DESCRIPTION

The 82S140 and 82S141 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S140 and 82S141 are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 4 chip enable inputs for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S140 and 82S141 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S140/141, F, and for the military temperature range (-55°C to +125°C) specify S82S140/141, F.

## FEATURES

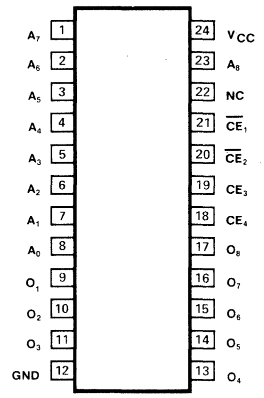
- **Address access time:**
  **N82S140/141: 60ns max**
  **S82S140/141: 90ns max**
- **Power dissipation: .17mW/bit typ**
- **Input loading:**
  **N82S140/141: -100μA max**
  **S82S140/141: -150μA max**
- **On-chip address decoding**
- **Output options:**
  **S82S140: Open collector**
  **S82S141: Tri-state**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

## APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

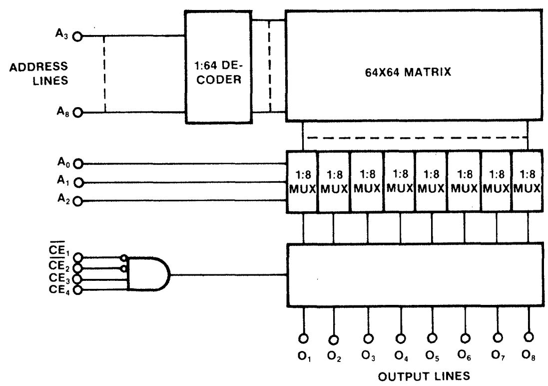
## PIN CONFIGURATION

F,N PACKAGE *




*F = Cerdip
N = Plastic

## BLOCK DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | +7 | Vdc |
| $V_{IN}$ | Input voltage | +5.5 | Vdc |
| | Output voltage | | Vdc |
| $V_{OH}$ | High (82S140) | +5.5 | |
| $V_O$ | Off-state (82S141) | +5.5 | |
| | Temperature range | | °C |
| $T_A$ | Operating | | |
| | N82S140/141 | 0 to +75 | |
| | S82S140/141 | -55 to +125 | |
| $T_{STG}$ | Storage | -65 to +150 | |

## DC ELECTRICAL CHARACTERISTICS

N82S140/141: 0°C ≤ $T_A$ ≤ +75°C, 4.75V ≤ $V_{CC}$ ≤ 5.25V
S82S140/141: -55°C ≤ $T_A$ ≤ +125°C, 4.5V ≤ $V_{CC}$ ≤ 5.5V

| PARAMETER | | TEST CONDITIONS[1] | N82S140/141 | | | S82S140/141 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[2] | Max | Min | Typ[2] | Max | |
| | Input voltage | | | | | | | | V |
| $V_{IL}$ | Low | | | | .85 | | | .80 | |
| $V_{IH}$ | High | | 2.0 | | | 2.0 | | | |
| $V_{IC}$ | Clamp | $I_{IN}$ = -18mA | | -0.8 | -1.2 | | -0.8 | -1.2 | |
| | Output voltage | | | | | | | | V |
| $V_{OL}$ | Low | $I_{OUT}$ = 9.6mA | | | 0.45 | | | 0.5 | |
| $V_{OH}$ | High (82S141) | $\overline{CE}_1$ = Low, $I_{OUT}$ = -2mA, $\overline{CE}_2$ = Low, $CE_3$ = High, $CE_4$ = High, High stored | 2.4 | | | 2.4 | | | |
| | Input current | | | | | | | | µA |
| $I_{IL}$ | Low | $V_{IN}$ = 0.45V | | | -100 | | | -150 | |
| $I_{IH}$ | High | $V_{IN}$ = 5.5V | | | 40 | | | 50 | |
| | Output current | | | | | | | | |
| $I_{OLK}$ | Leakage (82S140) | $\overline{CE}_1$ = High, $V_{OUT}$ = 5.5V, $\overline{CE}_2$ = High, $CE_3$ = Low, $CE_4$ = Low | | | 40 | | | 60 | µA |
| $I_{O(OFF)}$ | Hi-Z state (82S141) | $\overline{CE}_1$ = High, $V_{OUT}$ = 0.5V, $\overline{CE}_2$ = High, $CE_3$ = Low, $CE_4$ = Low | | | -40 | | | -60 | µA |
| | | $\overline{CE}_1$ = High, $V_{OUT}$ = 5.5V, $\overline{CE}_2$ = High, $CE_3$ = Low, $CE_4$ = Low | | | 40 | | | 60 | |
| $I_{OS}$ | Short circuit (82S141) | $V_{OUT}$ = 0V | -20 | | -70 | -15 | | -85 | mA |
| $I_{CC}$ | $V_{CC}$ supply current | | | 140 | 175 | | 140 | 185 | mA |
| | Capacitance | $V_{CC}$ = 5.0V | | | | | | | pF |
| $C_{IN}$ | Input | $V_{IN}$ = 2.0V | | 5 | | | 5 | | |
| $C_{OUT}$ | Output | $V_{OUT}$ = 2.0V | | 8 | | | 8 | | |

## AC ELECTRICAL CHARACTERISTICS

$R_1$ = 470Ω, $R_2$ = 1kΩ, $C_L$ = 30pF
N82S140/141: 0°C ≤ $T_A$ ≤ +75°C, 4.75V ≤ $V_{CC}$ ≤ 5.25V
S82S140/141: -55°C ≤ $T_A$ ≤ +125°C, 4.5V ≤ $V_{CC}$ ≤ 5.5V

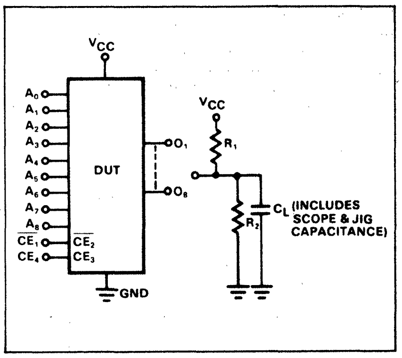
| PARAMETER | | TO | FROM | N82S140/141 | | | S82S140/141 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[2] | Max | Min | Typ[2] | Max | |
| | Access time | | | | | | | | | ns |
| $T_{AA}$ | | Output | Address | | 40 | 60 | | 40 | 90 | |
| $T_{CE}$ | | Output | Chip enable | | 20 | 40 | | 20 | 50 | |
| | Disable time | | | | | | | | | ns |
| $T_{CD}$ | | Output | Chip disable | | 20 | 40 | | 20 | 50 | |

NOTES

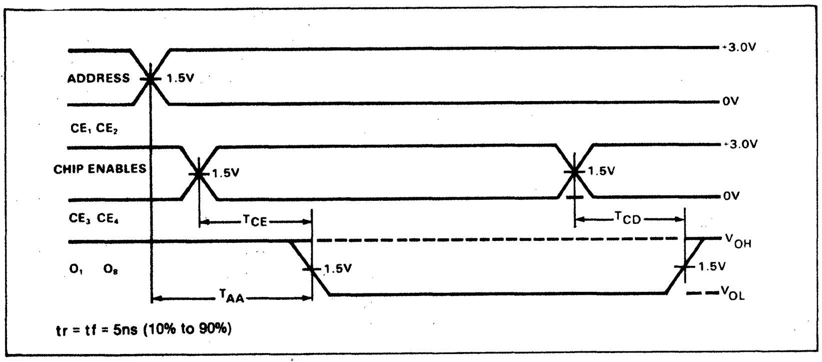
1. Positive current is defined as into the terminal referenced.
2. Typical values are at $V_{CC}$ = 5.0V, $T_A$ = +25°C.

BIPOLAR MEMORY

## TEST LOAD CIRCUIT




## VOLTAGE WAVEFORM




## PROGRAMMING SYSTEMS SPECIFICATIONS

(Testing of these limits may cause programming of device.) $T_A$ = +25°C

| | PARAMETER | TEST CONDITIONS | LIMITS Min | Typ | Max | UNIT |
|---|---|---|---|---|---|---|
| | Power supply voltage | | | | | V |
| $V_{CCP}$ | To program[1] | $I_{CCP}$ = 375 ± 75mA, Transient or steady state | 8.5 | 8.75 | 9.0 | |
| | Verify limit | | | | | V |
| $V_{CCH}$ | Upper | | 5.3 | 5.5 | 5.7 | |
| $V_{CCL}$ | Lower | | 4.3 | 4.5 | 4.7 | |
| $V_S$ | Verify threshold[2] | | 1.4 | 1.5 | 1.6 | V |
| $I_{CCP}$ | Programming supply current | $V_{CCP}$ = +8.75 ± .25V | 300 | | 450 | mA |
| | Input voltage | | | | | V |
| $V_{IH}$ | High | | 2.4 | | 5.5 | |
| $V_{IL}$ | Low | | 0 | 0.4 | 0.8 | |
| | Input current | | | | | μA |
| $I_{IH}$ | High | $V_{IH}$ = +5.5V | | | 50 | |
| $I_{IL}$ | Low | $V_{IL}$ = +0.4V | | | -500 | |
| $V_{OUT}$ | Output programming voltage[3] | $I_{OUT}$ = 200 ± 20mA, Transient or steady state | 16.0 | 17.0 | 18.0 | V |
| $I_{OUT}$ | Output programming current | $V_{OUT}$ = +17 ± 1V | 180 | 200 | 220 | mA |
| $T_R$ | Output pulse rise time | | 10 | | 50 | μs |
| $t_p$ | CE programming pulse width | | 0.3 | 0.4 | 0.5 | ms |
| $t_D$ | Pulse sequence delay | | 10 | | | μs |
| $T_{PR}$ | Programming time | $V_{CC} = V_{CCP}$ | | | 12 | sec |
| $T_{PSI}$ | Initial programming pause | $V_{CC}$ = 0V | 6 | | | sec |
| $\frac{T_{PR}}{T_{PR}+T_{PS}}$ | Programming duty cycle[4] | | | | 50 | % |
| $F_L$ | Fusing attempts per link | | | | 2 | cycle |

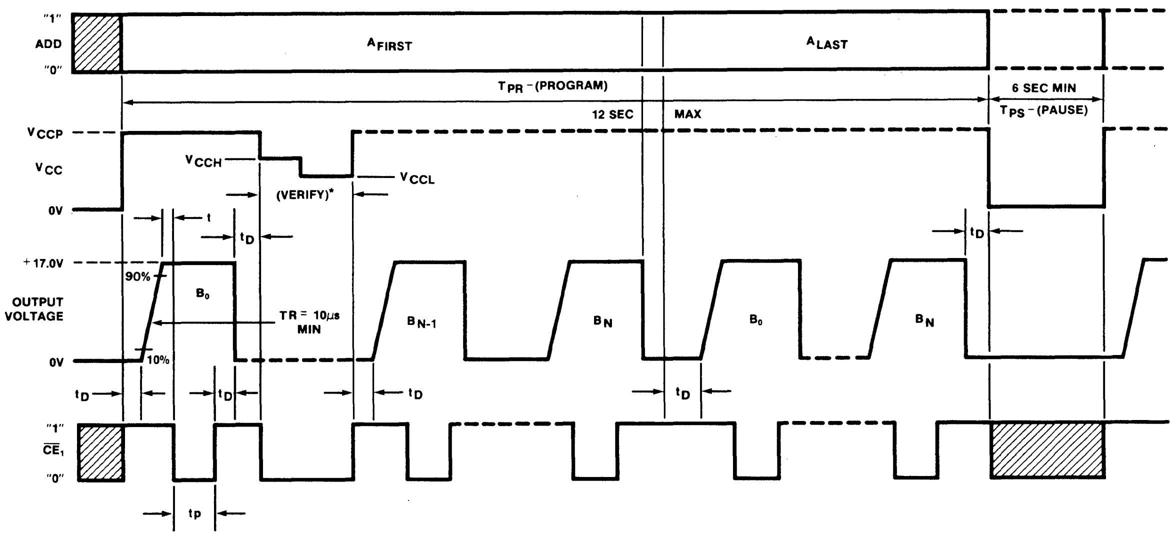
NOTES

1. Bypass $V_{CC}$ to GND with a 0.01μF capacitor to reduce voltage spikes.
2. $V_S$ is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. Care should be taken to insure the 17 ± 1V output voltage is maintained during the entire fusing cycle.
4. Programming duty cycle is 50% after continuous programming at 100% duty cycle.
5. This is an updated method of programming and does not obsolete any programming systems presently being used.

## PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10kΩ resistor to $V_{CC}$. Apply $\overline{CE}_1$ = High, $\overline{CE}_2$ = Low, $CE_3$ = High and $CE_4$ = High.
2. Select the Address to be programmed, and raise $V_{CC}$ to $V_{CCP}$ = 8.75 ± .25V.
3. After 10μs delay, apply $V_{OUT}$ = +17 ± 1V to the output to be programmed. Program one output at the time.
4. After 10μs delay, pulse the $\overline{CE}_1$ input to logic low for 0.3 to 0.5ms.
5. After 10μs delay, remove +17V from the programmed output.
6. To verify programming, after 10μs delay, lower $V_{CC}$ to $V_{CCH}$ = +5.5 ± .2V, and apply a logic low level to the CE input. The programmed output should remain in the high state. Again, lower $V_{CC}$ to $V_{CCL}$ = +4.5 ± .2V, and verify that the programmed output remains in the high state.
7. Raise $V_{CC}$ to $V_{CCP}$ = 8.75 ± .25V, and repeat steps 3 through 6 to program other bits at the same address.
8. After 10μs delay, repeat steps 2 through 7 to program all other address locations.

## TYPICAL PROGRAMMING SEQUENCE




*Programming verification at both high and low $V_{CC}$ margins is optional. For convenience, verification can also be executed at the operating $V_{CC}$ limits specified in the dc characteristics.