93448 ✓

ISOPLANAR SCHOTTKY TTL MEMORY

512×8-BIT PROGRAMMABLE READ ONLY MEMORY

01C771

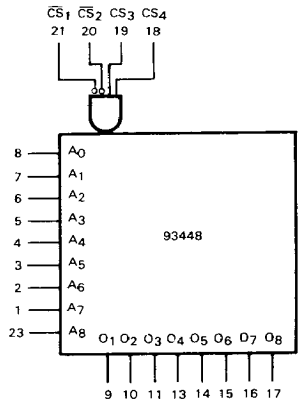
DESCRIPTION – The 93448 is a fully decoded 4096-bit field Programmable ROM organized 512 words by eight bits per word. The 93448 has 3-state outputs. The device is enabled when $\overline{CS}_1$ and $\overline{CS}_2$ are LOW and CS_3 and CS_4 are HIGH. The 93448 is supplied with all bits stored as logic "1"s and may be programmed to logic "0"s by following the field programming procedure.

- FULL MIL AND COMMERCIAL RANGES
- FIELD PROGRAMMABLE
- ORGANIZATION – 512 WORDS X 8 BITS
- 3-STATE OUTPUTS
- FULLY DECODED – ON-CHIP ADDRESS DECODER AND BUFFER
- CHIP SELECT INPUTS PROVIDE EASY MEMORY EXPANSION
- WIRED-OR CAPABILITY
- STANDARD 24-PIN DUAL IN-LINE PACKAGE
- NICHROME FUSE LINKS FOR HIGH RELIABILITY
- REPLACES TWO 256 X 8 PROMs – DOUBLE DENSITY WITH SAME SPACE AND POWER

PIN NAMES

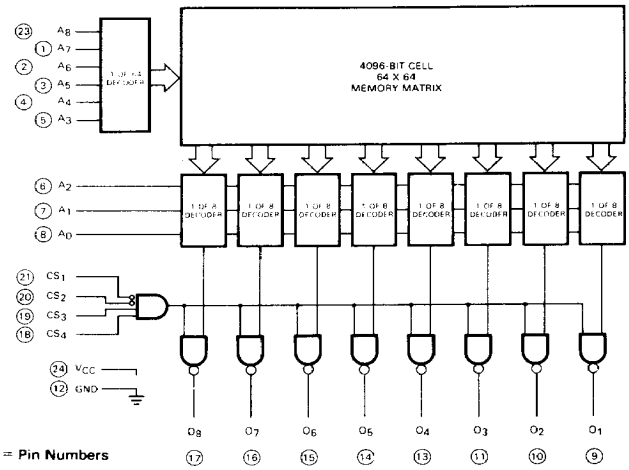
$\overline{A_0} - \overline{A_8}$	Address Inputs
$\overline{CS}_1, \overline{CS}_2, CS_3, CS_4$	Chip Select Inputs
$O_1 - O_8$	Data Outputs

LOGIC SYMBOL

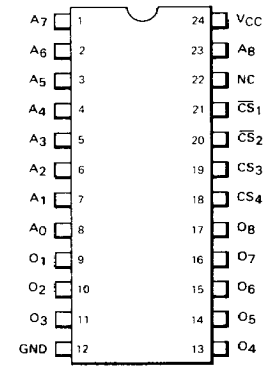


V_{CC} = Pin 24
GND = Pin 12

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC}	−0.5 V to +7.0 V
Input Voltage	−0.5 V to +5.5 V
Current into Output Terminal	100 mA
Output Voltages	−0.5 V to 4.0 V

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE
	MIN	TYP	MAX	
93448XC·	4.75 V	5.0 V	5.25 V	0°C to +75°C
93448XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

FUNCTIONAL DESCRIPTION – The 93448 is a bipolar field Programmable Read Only Memory (PROM) organized 512 words by eight bits per word. The 93448 has 3-state outputs which provide active pull-ups when enabled and high output impedance when disabled. Chip Select for both devices follows the logic equation: $\overline{CS}_1 \bullet \overline{CS}_2 \bullet CS_3 \bullet CS_4 = CS$; i.e., if $\overline{CS}_1$ and $\overline{CS}_2$ are both active LOW and CS_3 and CS_4 are both active HIGH, all eight outputs are enabled; for any other condition all eight outputs are disabled.

The read function is identical to that of a conventional bipolar ROM. That is, a binary address is applied to the A_0 through A_8 inputs, the chip is selected, and data is valid at the outputs after t_{AA} nanoseconds.

Programming (selectively opening nichrome fuse links) is accomplished by following the procedures in Chapter 6, page 6-14.

DC CHARACTERISTICS: Over guaranteed operating ranges unless otherwise note.

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA A_0 = +10.8 V, $A_1 - A_8$ = HIGH
V_{OH}	Output HIGH Voltage	2.4			V	V_{CC} = MIN, I_{OH} = −2.0 mA
I_{off}	Output Leakage Current for HIGH Impedance State			50 −50	µA µA	V_{OH} = 2.4 V V_{OL} = 0.4 V — 0°C to +75°C
I_{off}	Output Leakage Current for HIGH Impedance State			100 −50	µA µA	V_{OH} = 2.4 V V_{OL} = 0.4 V — −55°C to +125°C
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
I_F	Input LOW Current I_{FA} (Address Inputs) I_{FCS} (Chip Select Inputs)		−160 −160	−250 −250	µA µA	V_{CC} = MAX, V_F = 0.45 V
I_R	Input HIGH Current I_{RA} (Address Inputs) I_{RCS} (Chip Select Input)			40 40	µA µA	V_{CC} = MAX, V_R = 2.4 V
I_{CC}	Power Supply Current		130	175	mA	V_{CC} = MAX, Outputs Open Inputs Grounded and Chip Selected
C_O	Output Capacitance		7		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
C_{IN}	Input Capacitance		4		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
V_C	Input Clamp Diode Voltage			−1.2	V	V_{CC} = MIN, I_A = −18 mA

AC CHARACTERISTICS: T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%

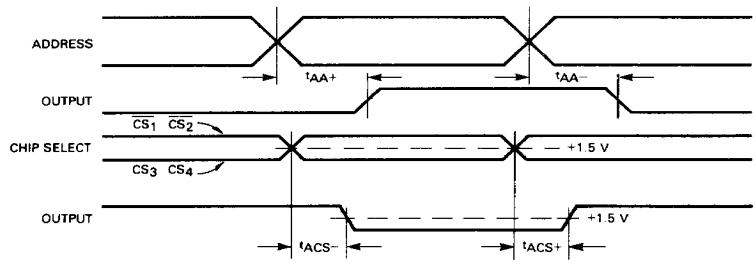
SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
t_{AA-} t_{AA+}	Address to Output Access Time		35 35	55 55	ns ns	See Waveforms and Test Circuits
t_{ACS-} t_{ACS+}	Chip Select Access Time		15 15	25 25	ns ns	

AC CHARACTERISTICS: T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%

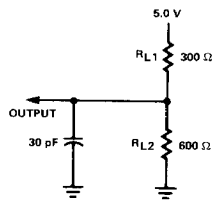
SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
t_{AA-} t_{AA+}	Address to Output Access Time		35 35	70 70	ns ns	See Waveforms and Test Circuits
t_{ACS-} t_{ACS+}	Chip Select Access Time		15 15	30 30	ns ns	

Note (1): Typical values are at V_{CC} = 5.0 V, 5.0 V, +25°C and max loading.

SWITCHING WAVEFORMS



SWITCHING TEST OUTPUT LOAD



15 mA Load

Fig. 1