FUJITSU

CMOS 2M-BIT MASK-PROGRAMMABLE READ ONLY MEMORY

MB832000

April 1988
Edition 1.0

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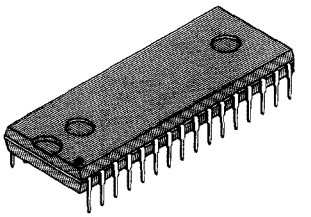
2M-BIT(262,144 x 8) CMOS READ ONLY MEMORY

The Fujitsu MB832000 is a CMOS Si-gate mask-programmable static read only memory organized as 262,144 words by 8 bits.

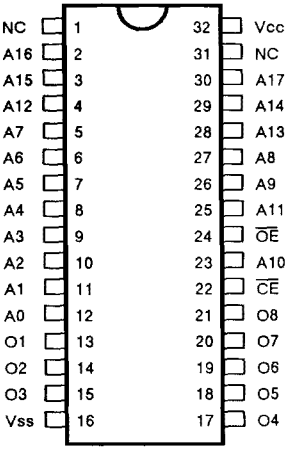
The MB832000 has TTL-compatible I/O and 3-state output level with fully-static operation (i.e. no need of clock signal) and a single +5V power supply is required. Also, the MB832000 is designed for applications such as character generator or program storage which require large memory capacity and high-speed/low-power operation.

- Organization: 262,144 words x 8 bits
- Access time: 200 ns
- Completely static operation: No clock required
- TTL compatible Input/Output
- Three state ouput
- Single +5V power supply
- Power dissipation:
  220 mW max. (Active)
  16.5mW max. (Standby, TTL input level)
  275 µW max. (Standby, CMOS input level)
- 32-pin DIP(Pin compatible with MBM27C1001)



PLASTIC PACKAGE
DIP-32P-M01

PIN ASSIGNMENT
MB832000



ABSOLUTE MAXIMUM RATINGS (see NOTE)

(Referenced to GND)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.5 to VCC+0.5	V
Output Voltage	V_{OUT}	-0.5 to VCC+0.5	V
Temperature Under Bias	T_{BIAS}	-10 to +85	°C
Storage Temperature Range	T_{STG}	-45 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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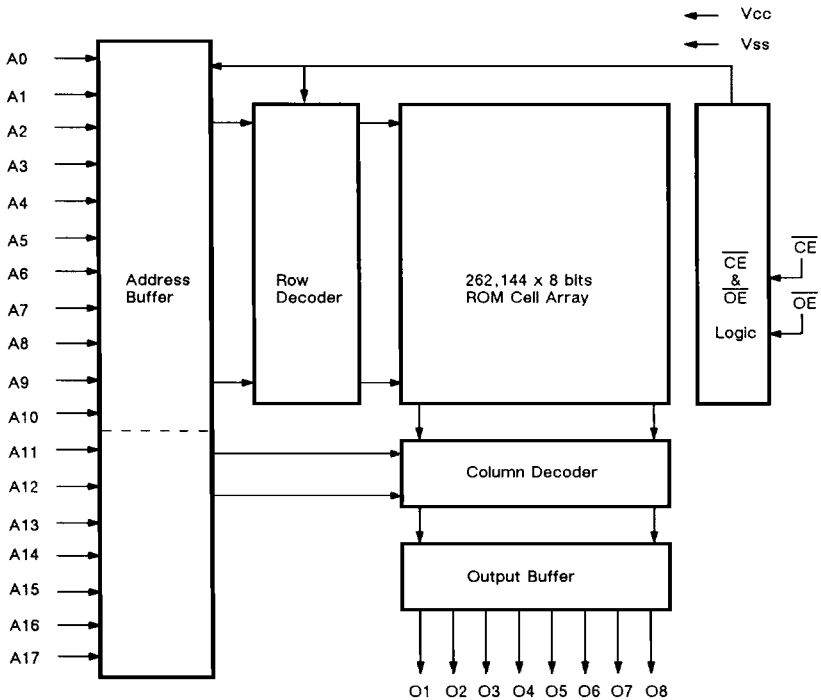
Fig. 1-MB832000 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	Mode	Output	Power Mode
H	X	Not Selected	High-Z	Standby
L	H	Not Selected	High-Z	Active
L	L	Selected	Data Out	Active

CAPACITANCE (TA=25°C, f=1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Output Capacitance (VOUT=0V)	C_{OUT}			15	pF
Input Capacitance (VIN=0V)	C_{IN}			10	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Input Low Voltage	VIL	-0.3		0.8	V
Input High Voltage	VIH	2.2		VCC+0.3	V
Ambient Temperature	TA	0		70	°C

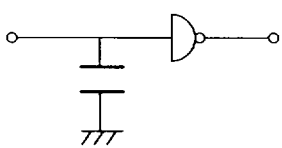
DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Active Supply Current	$\overline{CE}$=VIL, Min. Cycle	ICC			40	mA
Standby Supply Current	$\overline{CE}$=VIH	ISB1			3	mA
	$\overline{CE}$=VIH=VCC, VIN=VSS or VCC	ISB2			50	µA
Input Leakage Current	VIN=0 to VCC	ILI	-10		10	µA
Output Leakage Current	$\overline{CE}$=VIH, $\overline{OE}$=VIH	ILO	-10		10	µA
Output High Voltage	IOH=-400µA	VOH	2.4			V
Output Low Voltage	IOL=2.1mA	VOL			0.4	V

Fig. 2 - AC TEST CONDITION

- Input Pulse Level : 0.6 to 2.4V
- Input Pulse Rise and Fall Time : tT=5ns
- Timing Reference Levels : Input VIL=0.8V, VIH=2.2V
  Output VOL=0.8V, VOH=2.2V
- Output Load : 1 TTL Gate and 100pF



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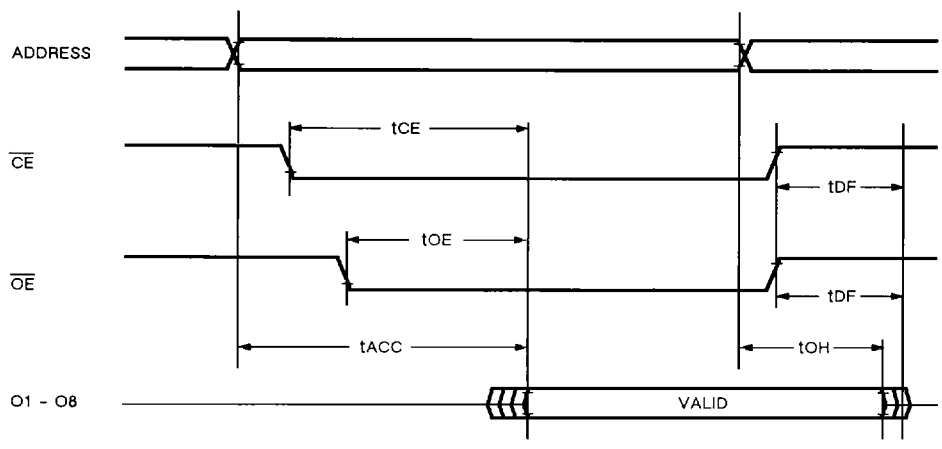
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Address Access Time	tACC	$\overline{CE}$=$\overline{OE}$=VIL			200	ns
$\overline{CE}$ Access Time	tCE	$\overline{OE}$=VIL			200	ns
$\overline{OE}$ Access Time	tOE	Note 1			100	ns
Output Disable Time	tDF	Note 2			60	ns
Output Hold Time	tOH	$\overline{CE}$=$\overline{OE}$=VIL	0			ns

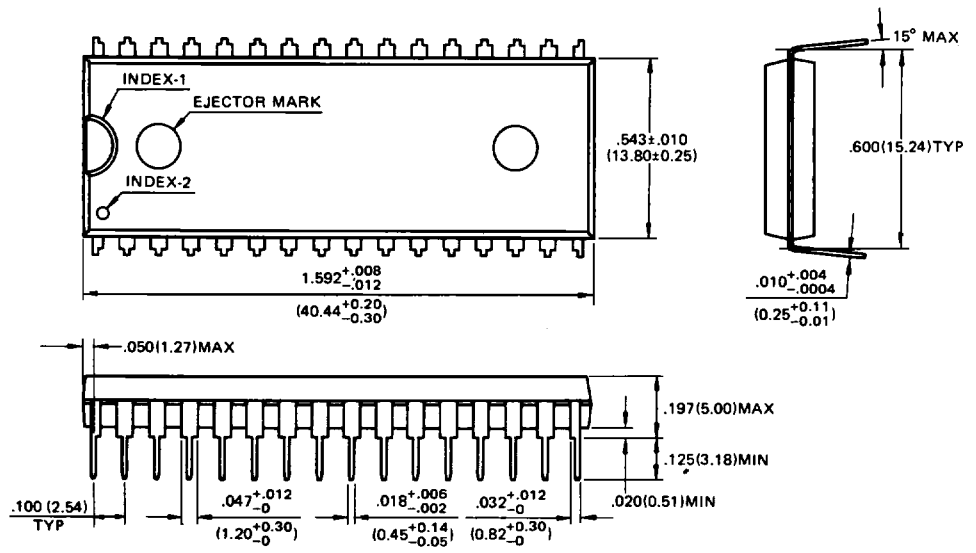
Note 1: $\overline{OE}$ may be delayed up to (tACC-tOE) after the falling edge of $\overline{CE}$ without impact on tACC.
Note 2: tDF is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs earlier.

TIMING DIAGRAM



PACKAGE DIMENSIONS

32-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-32P-M01)



Dimensions in
inches (millimeters)

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