μPD27C1000A
131,072 x 8-BIT
CMOS UV EPROM

Description

The μPD27C1000A is a 1,048,576-bit ultraviolet erasable and electrically programmable read-only memory fabricated with double-polysilicon CMOS technology for a substantial savings in both operating and standby power. The device is organized as 131,072 words by 8 bits and operates from a single +5-volt power supply.

The μPD27C1000A has both page and single-location programming features, three-state outputs, and fully TTL-compatible inputs and outputs. It also has a program voltage (V_{PP}) of 12.5 volts and is available in a 32-pin cerdip with a quartz window.

Features

- ☐ 131,072-word by 8-bit organization
- ☐ Ultraviolet erasable and electrically programmable
- ☐ High-speed programming capability
  - — Page programming
  - — Single byte programming
- ☐ Low power dissipation
  - — 40 mA maximum (active)
  - — 100 μA maximum (standby)
- ☐ TTL-compatible I/O for reading and programming
- ☐ Single +5-volt power supply
- ☐ Double-polysilicon CMOS technology
- ☐ 32-pin cerdip packaging
- ☐ Pinout compatibility with 28-pin, mask-programmable μPD23C1000s

Ordering Information

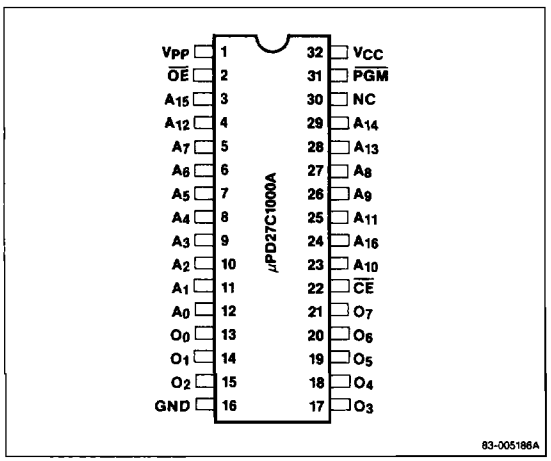
Part Number	Access Time (max)	Package
μPD27C1000AD-12	120 ns	32-pin cerdip with a quartz window
D-15	150 ns	
D-20	200 ns	

Pin Identification

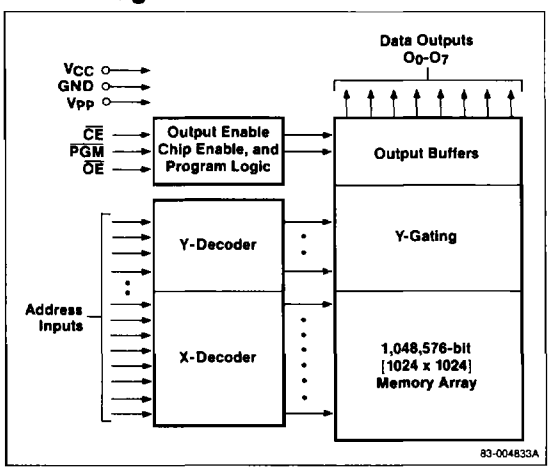
Symbol	Function
A_0-A_{16}	Address inputs
O_0-O_7	Data outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{PGM}$	Program
GND	Ground
V_{CC}	+5-volt power supply
V_{PP}	Program voltage
NC	No connection

Pin Configuration

32-Pin Cerdip



Block Diagram



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Absolute Maximum Ratings

Power supply voltage, V_{CC}	−0.6 to +7.0 V
Input voltage, V_{IN}	−0.6 to +7.0 V
Input voltage, A_9	−0.6 to +13.5 V
Output voltage, V_{OUT}	−0.6 to +7.0 V
Operating temperature, T_{OPR}	−10 to +80°C
Storage temperature, T_{STG}	−65 to +125°C
Program voltage, V_{PP}	−0.6 to +13.5 V

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}			14	pF	V_{IN} = 0 V
Output capacitance	C_{OUT}			16	pF	V_{OUT} = 0 V

Truth Table

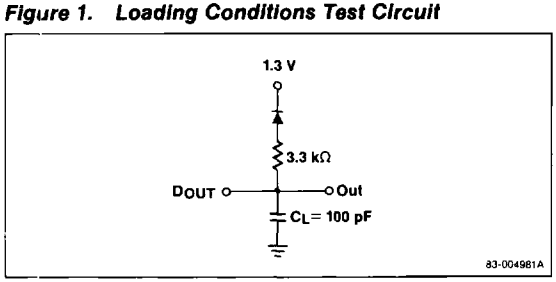
Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$ (Note 2)	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	+5.0 V	+5.0 V	D_{OUT}
Output disable	V_{IL}	V_{IH}	X	+5.0 V	+5.0 V	High-Z
Standby	V_{IH}	X	X	+5.0 V	+5.0 V	High-Z
Page data latch	V_{IH}	V_{IL}	V_{IH}	+12.5 V	+6.5 V	D_{IN}
Page program	V_{IH}	V_{IH}	V_{IL}	+12.5 V	+6.5 V	High-Z
Program verify	V_{IL}	V_{IL}	V_{IH}	+12.5 V	+6.5 V	D_{OUT}
Byte program	V_{IL}	V_{IH}	V_{IL}	+12.5 V	+6.5 V	D_{IN}
Program inhibit	X	V_{IL}	V_{IL}	+12.5 V	+6.5 V	High-Z
	X	V_{IH}	V_{IH}			

Notes:

(1) "X" can be either V_{IL} or V_{IH}.

(2) In read operation, $\overline{PGM}$ must be set to V_{IH} at all times or switched from V_{IL} to V_{IH} at least 2 μs before $\overline{OE}$ or $\overline{CE}$ becomes V_{IH}.

Figure 1. Loading Conditions Test Circuit



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; V_{PP} = V_{CC} ±0.6

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Read, Output Disable, and Standby Modes						
Output voltage, high	V_{OH1}	2.4			V	I_{OH} = −400 μA
	V_{OH2}	V_{CC} − 0.7			V	I_{OH} = −100 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input voltage, high	V_{IH}	2.0		V_{CC} + 0.3	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
Output leakage current	I_{LO}	−10		10	μA	$\overline{OE}$ = V_{IH}; V_{OUT} = 0 V to V_{CC}
Input leakage current	I_{LI}	−10		10	μA	V_{IN} = 0 V to V_{CC}
Operating supply current	I_{CCA1}			15	mA	$\overline{CE}$ = V_{IL}; V_{IN} = V_{IH}
	I_{CCA2}			40	mA	f = 8.4 MHz; t_{ACC} = 120 ns; I_{OUT} = 0 mA
				30	mA	f = 6.7 MHz; t_{ACC} = 150 ns; I_{OUT} = 0 mA
				25	mA	f = 5 MHz; t_{ACC} = 200 ns; I_{OUT} = 0 mA
Standby supply current	I_{CCS1}			1	mA	$\overline{CE}$ = V_{IH}
	I_{CCS2}		1	100	μA	$\overline{CE}$ = V_{CC}; V_{IN} = 0 V to V_{CC}
Program voltage current	I_{PP}		1	100	μA	V_{PP} = V_{CC}
All Program Modes						
T_A = +25 ±5°C; V_{CC} = +6.5 ±0.25 V; V_{PP} = +12.5 ±0.3 V						
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −400 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input voltage, high	V_{IH}	2.4		V_{CC} + 0.3	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
Input leakage current	I_{LI}	−10		10	μA	V_{IN} = V_{IL} or V_{IH}
Operating supply current	I_{CC}			30	mA	
Program voltage current	I_{PP}			50	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; V_{PP} = V_{CC}

Parameter	Symbol	Limits μPD27C1000A-12 Min	Limits μPD27C1000A-12 Max	Limits μPD27C1000A-15 Min	Limits μPD27C1000A-15 Max	Limits μPD27C1000A-20 Min	Limits μPD27C1000A-20 Max	Unit	Test Conditions
Read and Standby Modes									
Address to output delay	t_{ACC}		120		150		200	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to output delay	t_{CE}		120		150		200	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to output delay	t_{OE}		70		70		75	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ or $\overline{CE}$ high to data output float delay	t_{DF}	0	50	0	50	0	60	ns	$\overline{CE} = V_{IL}$ or $\overline{OE} = V_{IL}$
Address to output hold time	t_{OH}	0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

Notes:

(1) See figure 1 for output load; input rise and fall times ≤ 20 ns; input pulse levels = 0.45 V and 2.4 V; input and output timing measurement levels = 0.8 V and 2.0 V.

AC Characteristics (cont)

T_A = +25 ±5°C; V_{CC} = +6.5 ±0.25 V; V_{PP} = +12.5 ±0.3 V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions (Note 1)
Page Data Latch, Page Program, Program Verify, and Program Inhibit Modes						
Address setup time	t_{AS}	2			μs	
Data setup time	t_{DS}	2			μs	
Address hold time	t_{AH}	2			μs	
	t_{AHL}	2			μs	
	t_{AHV}	0			μs	
Data hold time	t_{DH}	2			μs	
Output enable to output float delay	t_{DF}	0		130	ns	
V_{PP} setup time	t_{VPS}	2			μs	
Program pulse width	t_{PW}	0.095	0.1	0.105	ms	
V_{CC} setup time	t_{VCS}	2			μs	
$\overline{OE}$ setup time	t_{OES}	2			μs	
$\overline{OE}$ hold time	t_{OEH}	2			μs	
$\overline{CE}$ hold time	t_{CEH}	2			μs	
$\overline{OE}$ pulse width during data latch	t_{LW}	1			μs	
$\overline{PGM}$ setup time	t_{PGMS}	2			μs	
$\overline{CE}$ setup time	t_{CES}	2			μs	
Data valid from $\overline{OE}$	t_{OE}			150	ns	

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions (Note 1)
Byte Programming Mode						
Address setup time	t_{AS}	2			μs	
$\overline{OE}$ setup time	t_{OES}	2			μs	
Data setup time	t_{DS}	2			μs	
Address hold time	t_{AH}	2			μs	
Data hold time	t_{DH}	2			μs	
$\overline{OE}$ to output float time	t_{DF}	0		130	ns	
V_{PP} setup time	t_{VPS}	2			μs	
V_{CC} setup time	t_{VCS}	2			μs	
Initial program pulse width	t_{PW}	0.095	0.1	0.105	ms	
$\overline{CE}$ setup time	t_{CES}	2			μs	
$\overline{OE}$ to output delay	t_{OE}			150	ns	

Notes:

(1) Input pulse levels = 0.45 V to 2.4 V; input and output timing reference levels = 0.8 V and 2.0 V; input rise and fall times ≤ 20 ns. See figure 1 for output load.

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Programming Operation

Begin programming by erasing all data; this sets all bits at a high logic level (1). The μPD27C1000A is originally shipped in this condition. To enter data, program a low-level (0) TTL signal into the chosen location.

Address the first byte or page location and apply valid data at the eight output pins. Raise V_{CC} to +6.5 ±0.25 V; then raise V_{PP} to +12.5 ±0.3 V.

Byte Programming

For byte programming, $\overline{CE}$ should be set at 0 and $\overline{OE}$ at 1 to start programming at the initial address. Apply a 0.1-ms program pulse to $\overline{PGM}$ as shown in the byte programming portion of the timing waveforms. Set $\overline{OE}$ to 0 to verify the eight bits prior to making a program/no program decision. If the byte is not programmmed, apply another 0.1-ms pulse to $\overline{PGM}$, up to a maximum of 10 times, and input the next address. If the bits are not programmed in 10 tries, reject the device as a program failure.

After all addresses are programmed, lower both V_{CC} and V_{PP} to +5.0 V ±10% and verify all data again.

Page Programming

For page programming, $\overline{CE}$ and $\overline{PGM}$ should be set to 1. $\overline{OE}$ pulses low four times to latch the addressed 4-byte, one-page data. Subsequently, $\overline{CE}$ and $\overline{OE}$ should be set to a high level and a 0.1-ms program pulse applied to $\overline{PGM}$ as shown in the page programming portion of the timing waveforms. Verify the data prior to making a program/no program decision. If all four bytes of page data are not programmed, apply another 0.1-ms pulse to $\overline{PGM}$, up to a maximum of 10 times, and input the next page address. If the page is not programmed in 10 tries, reject the device as a program failure.

After all addresses are programmed, lower both V_{CC} and V_{PP} to +5.0 V ±10% and verify all data again.

Program Inhibit

Use the programming inhibit option to program multiple μPD27C1000As connected in parallel. All like inputs except $\overline{PGM}$ and $\overline{OE}$ may be common. Program individual devices by applying a low-level TTL pulse to the $\overline{PGM}$ pin of the device to be programmed. Applying a high-level signal to the $\overline{PGM}$ pins of the other devices prevents them from being programmed.

Program Verification

To verify that the device is correctly programmed, normal read operation can be used with a logic level 1 applied to the $\overline{PGM}$ pin and a logic level 0 applied to the $\overline{CE}$ and $\overline{OE}$ pins of the device to be verified. A logic level 1 should be applied to the $\overline{CE}$ and $\overline{OE}$ pins of all other devices.

Erasure

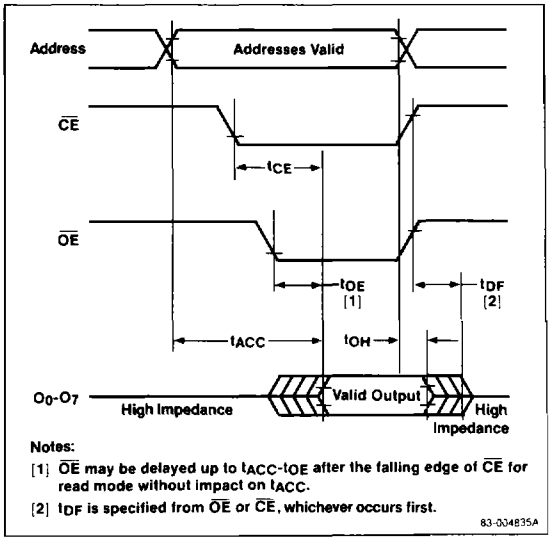
Erase data on the μPD27C1000A by exposing it to light with a wavelength shorter than 400 nm. Since exposure to direct sunlight or room-level fluorescent light could also erase the data, mask the window to prevent unintentional erasure by ultraviolet rays. Opaque labels are supplied with every device.

Data s typically erased by ultraviolet rays with a wavelength of 254 nm. A minimum integrated dose of 15 W-sec/cm^2 (ultraviolet lighting intensity multiplied by exposure time) is required to completely erase written data.

An ultraviolet lamp rated at 12,000 μW/cm^2 takes approximately 15 to 20 minutes to complete erasure. Place the μPD27C1000A within 2.5 cm of the lamp tubes and remove any filter on the lamp.

Timing Waveforms

Read Cycle



Notes:

[1] $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.

[2] t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

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Timing Waveforms (cont)

Page Programming

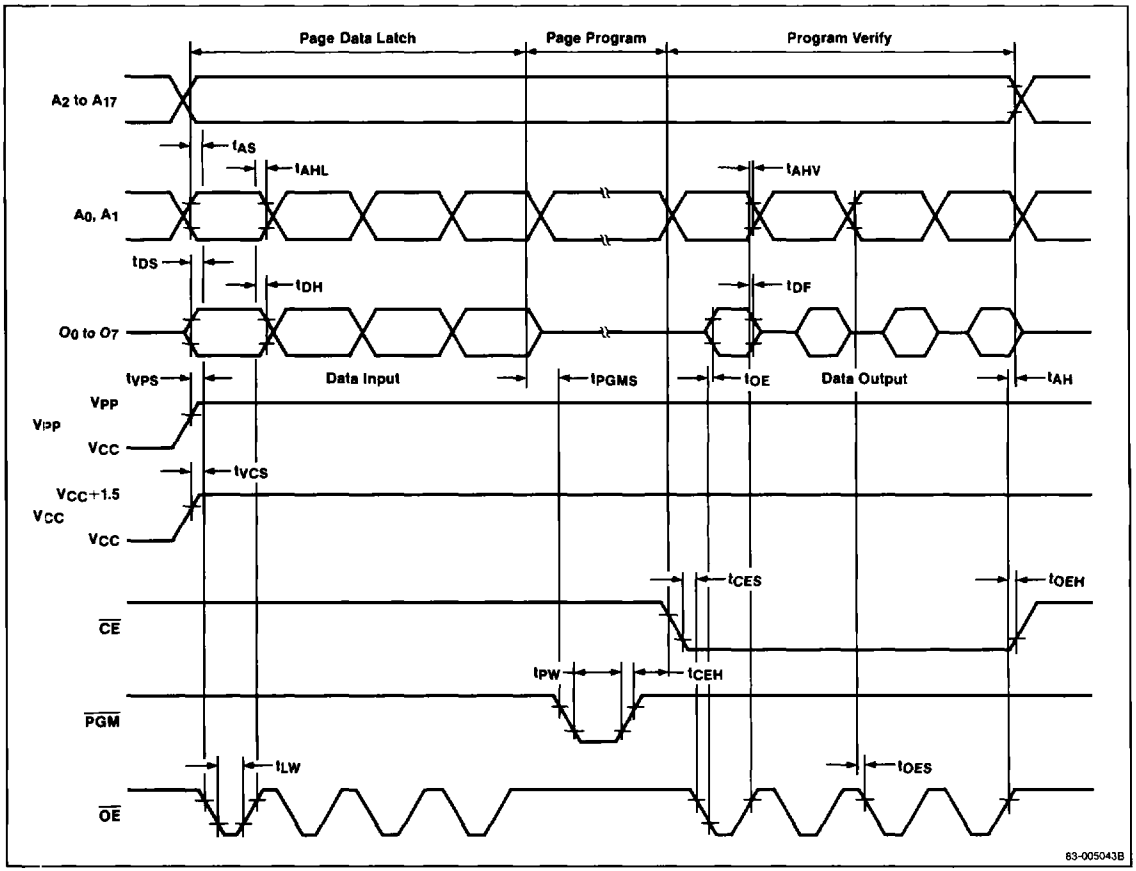
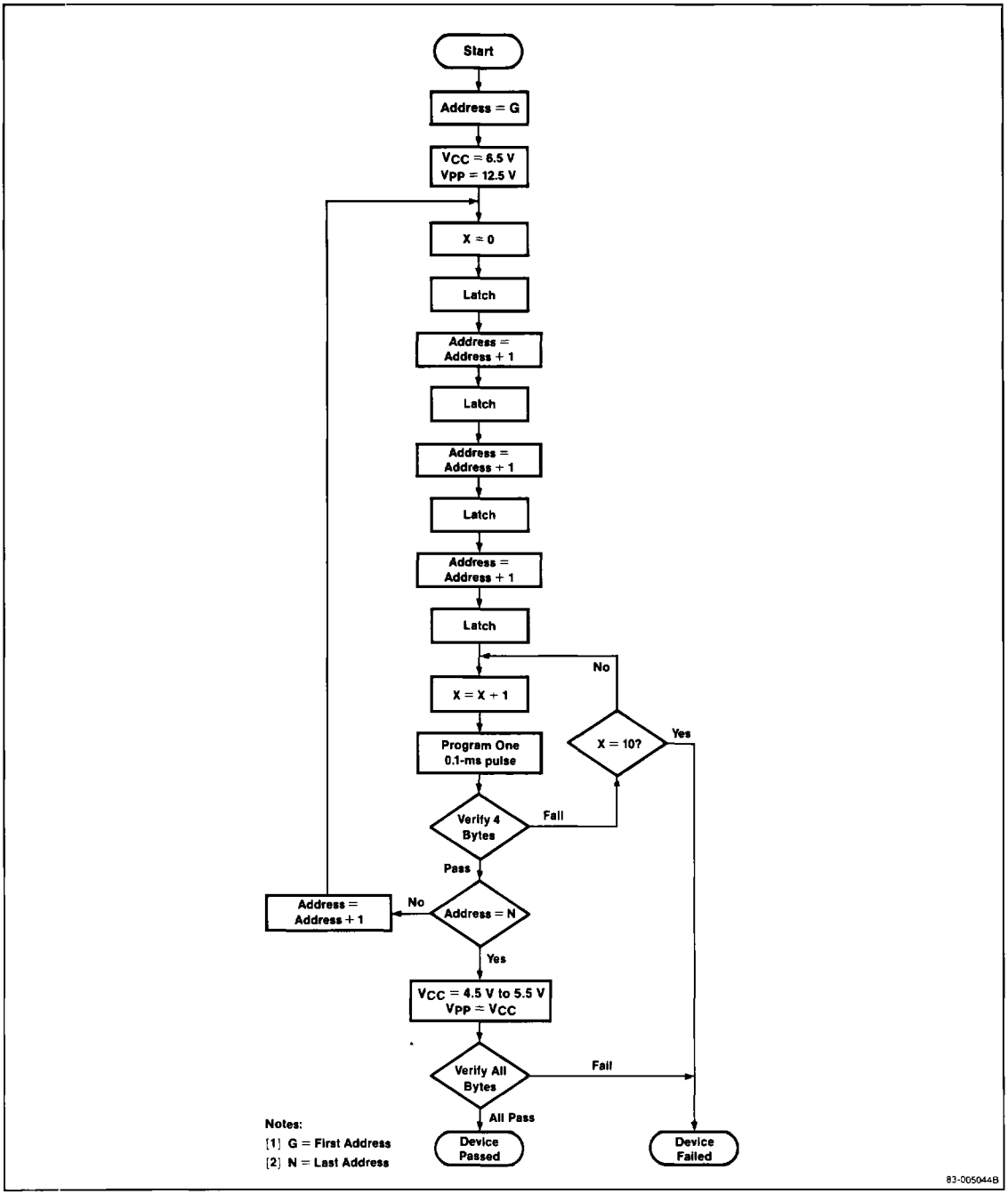


Figure 2. Page Programming Flowchart



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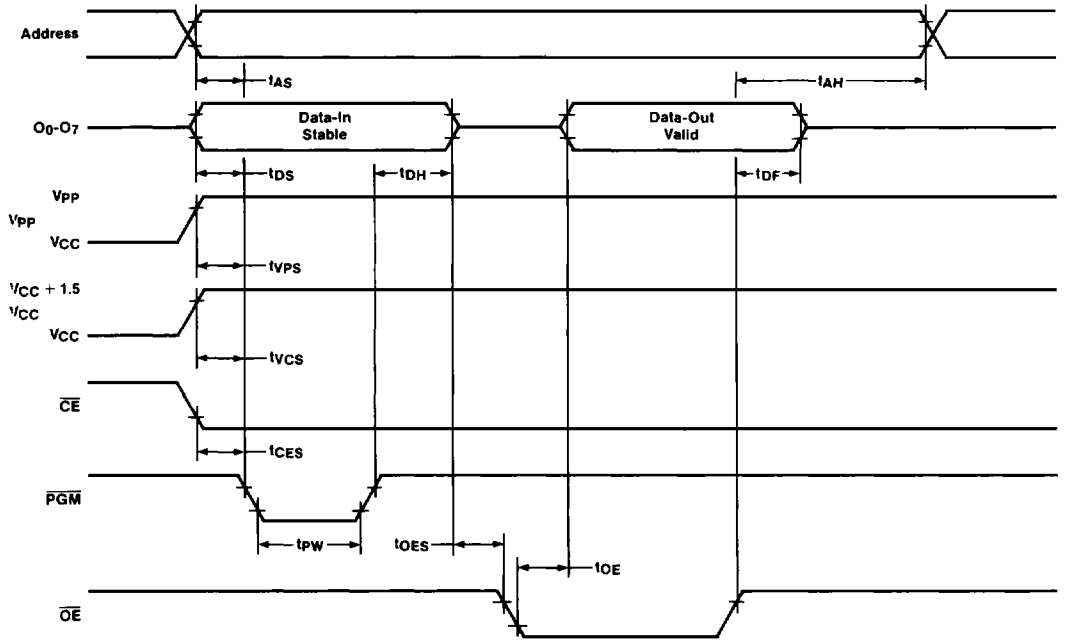
Timing Waveforms (cont)

Byte Programming



Notes:

[1] V_{CC} must be applied before or simultaneously with V_{PP} and removed after or simultaneously with V_{PP}.

[2] V_{PP} must not be greater than +13.5 V, including overshoot.

[3] Removing and reinserting the device while a voltage of 12.5 V is applied to V_{PP} may affect device reliability.

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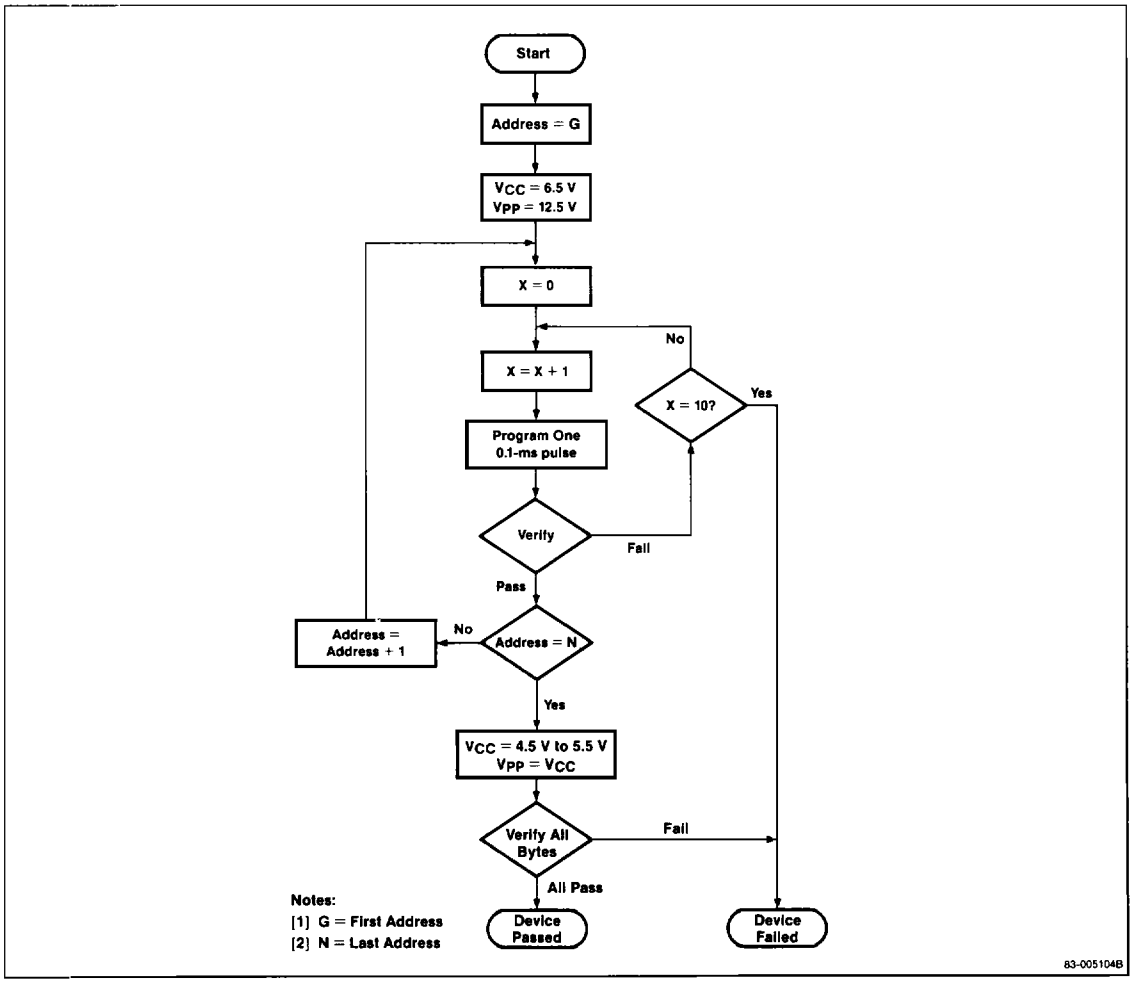
Figure 3. Byte Programming Flowchart



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