4096 WORD x 8 BIT MASK ROM

N CHANNEL SILICON GATE DEPLETION LOAD

TMM333P

DESCRIPTION

The TMM333P is a 32,768 bits read only memory organized as 4,096 words by 8 bits. It is suitable for use in programming of production apparatus used micro processor because of its low cost per bit.

The TMM333P's mask making is carried out by computer using punched paper tape data of customer and then sample manufacturing will start. Then for customer, 32,768 bits memory data and two chip select input active logic are programmable.

Therefore the TMM333P manufacturing procedure goes through three steps before mass production. First step is a acceptance of customer's punched paper tape data. Second step is a presentation of programmed sample (Engineering Sample) for customers. Third step is a verification of Engineering Sample by customers. Sample verification is most important and Toshiba will enter into mass production after above three steps are concluded. Then Toshiba will adopt a established on-line system and so can respond to a customer's needs quickly and can maintain a stable delivery.

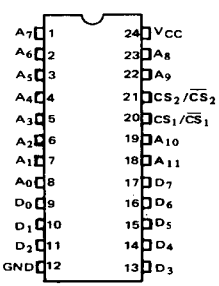
The TMM333P is fabricated with ion implanted N-channel silicon gate technology. This technology allows a production of high performance. The TMM 333P is moulded in a 24 pin standard plastic package.

FEATURES

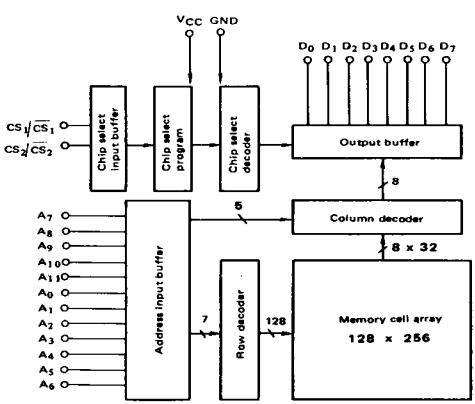
- Single 5V supply voltage; V_{CC} = 5V ± 5%
- Access time; t_{ACC} = 450 ns. (Max.)
- Directly TTL compatible; All inputs and outputs
- Programmable chip select inputs; CS1, CS2, Easy memory expansion
- Three state outputs; OR tie capability
- Static operation; No clocks are required.
- Input protected; All inputs have protection against static charge
- Pin to pin compatible; TMS4732

PIN CONNECTION

(TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_6$	Row address inputs
$A_7 \sim A_{11}$	Column address inputs
$D_0 \sim D_7$	Data outputs
$CS_1/\overline{CS_1}$; $CS_2/\overline{CS_2}$	Chip select inputs
VCC	Power supply terminal
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power supply voltage	−0.5 ~ 7.0	V
V_{IN}, V_{OUT}	Input and output voltage	−0.5 ~ 7.0	V
T_{opr}	Operating temperature	0 ~ 70	°C
T_{stg}	Storage temperature	−55 ~ 150	°C
T_{SOLDER}	Soldering temperature · time	260 · 10	°C · sec
P_D	Power Dissipation (Ta = 70°C)	1.0	W

D.C. OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input high voltage	–	2.0	–	V_{CC} + 1	V
V_{IL}	Input low voltage	–	−0.5	–	0.8	V
V_{CC}	Power supply voltage	–	4.75	5.0	5.25	V

D.C. and OPERATING CHARACTERISTICS (Ta = 0°C ~ 70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IH}	Input high current	$V_{IN} = V_{CC}$	–	0.01	10	μA
I_{IL}	Input low current	$V_{IN} = GND$	–	−0.01	−10	μA
V_{OH}	Output high voltage	$I_{SOURCE} = -0.4mA$	2.4	3.0	–	V
V_{OL}	Output low voltage	$I_{SINK} = 2.1mA$	–	0.2	0.4	V
I_{OH}	Output high current	$V_{OUT} = 2.4V$	−0.4	−3.0	–	mA
I_{OL}	Output low current	$V_{OUT} = 0.4V$	2.1	5.0	–	mA
I_{LO}	Output leakage current	$\overline{CS} = 0.8V$, $\overline{CS} = 2.0V$ $V_{OUT} = 0.4V$ to V_{CC}	–	±0.01	±10	μA
I_{CC}	Supply current	$I_{OUT} = 0mA$	–	60	100	mA

* Ta = 25°C, V_{CC} = 5V

A.C. CHARACTERISTICS ($Ta = 0°C \sim 70°C$, $V_{CC} = 5V \pm 5\%$, $C_L = 100pF$, $t_r, t_f = 20ns$)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.*	MAX.	UNIT
t_{ACC}	Access time	$t_{AC} \leqq 100ns$	–	300	450	ns
t_{CO}	Output delay time from chip select	$t_{AC} \geqq t_{ACC}$	–	120	200	ns
t_{OD}	Output deselect time	–	0	100	150	ns
t_{RC}	Read cycle time	–	450	–	–	ns

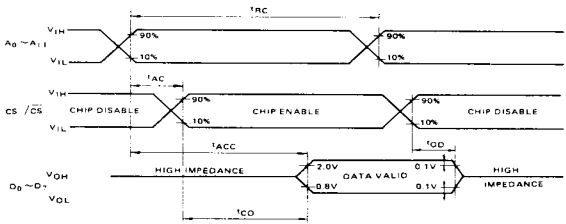
* Ta = 25°C, V_{CC} = 5V

CAPACITANCE (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input capacitance	V_{IN} = A. C. GND	–	4	10	pF
C_{OUT}	Output capacitance	V_{OUT} = A. C. GND	–	8	15	pF

Note: This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS



PAPER TAPE FORMAT

Punched paper tape data must be a positive logic and use a 7 to 8 bit ASCII code.
Format 1 (including Data and Check sum every word).

NULL	Take NULL more than fifty characters.
▼TMM333P - XXXX▼	Contents in single quotation mark (▼. . .▼) indicates a comment and XXXX is a user's number.
CR LF	CR and LF indicate carriage return and line feed respectively.
▼MSB = D_7▼	Specify MSB pin. (D_7 or D_0)
CR LF	
N8;	N8 indicates a 8-bit mask pattern. Semicolon (;) indicates a punctuation of data.
CR LF	
Ruuu0; X07P3; . . . . ; XF1P5;	R indicates an absolute address. Enter the address by decimal code every eight words.
CR LF	X indicates hexadecimal code. So enter the data represented by hexadecimal code every word after X.
. . . .	
CR LF	P indicates a check sum of its word. So enter a sum of one's number in a word by decimal code after P.
R4088; X01P1; . . . ; X3AP4;	Data modification: Enter the modified address before the End mark and then enter the data following above procedure independently or serialy. Modification can be allowed from 0 address to 4095 address.
CR LF	
(CS_1 = 0)	Customers can program the active logic of two chip select inputs independently. Specify the active logic of chip select input in the brackets. The example is shown in Figure. In this example, chip is active under the condition that CS1 = '0' and CS2 = '1'.
CR LF	
(CS_2 = 1)	
CR LF	
$	$ Indicates an End mark .
CR LF	
NULL	Take NULL more then fifty characters.

Format 2 (including Data only every word)

NULL
▼TMM333P - XXXX▼
CR LF
▼MSB = D_7 ▼
CR LF
N8;
CR LF
R0000; X075A . . . 38F1;
CR LF
.
.
.
R4080; XBCAE . . . 0085;
CR LF
(CS_1 = 0)
CR LF
(CS_2 = 0)
CR LF
$
CR LF
NULL

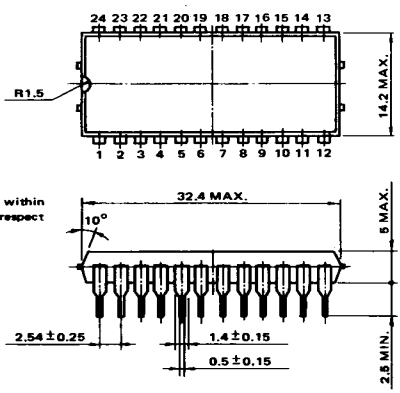
R indicates an absolute address. Enter the address by decimal code every sixteen words.

X indicates a hexadecimal code and so enter the data of sixteen words continuously after X.

Data modification: This procedure is following to Format 1. Otherwise specified in Format 1.

Format 1 and Format 2 are Toshiba preferred Format.
The other acceptable Format is Intel BNPF Format.

OUTLINE DRAWINGS



Note: Each lead pitch is 2.54 mm. All leads are located within 0.25 mm of their true longitudinal position with respect to No. 1 and No. 24 leads.
All dimensions are in millimeters.