VT2332/33 PRELIMINARY

4096 x 8 STATIC READ ONLY MEMORY

FEATURES

- 4096 x 8-bit organization
- Single +5 V supply
- Access Time—300 ns (max)
- Totally static operation
- Completely TTL compatible
- VT2332 pin compatible with 2532
- VT2333 pin compatible with 2732
- 3-State Outputs for wired-OR expansion
- Two programmable Chip Selects
- 2708/2716/2532/2732 EPROMs accepted as program data inputs

DESCRIPTION

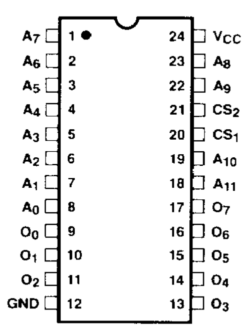
The VT2332/3 high-performance Read Only Memory is organized 4096 words by eight bits with access times of less than 300 ns. This ROM is designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. This device offers TTL input and output levels with a minimum of 0.4 V noise immunity in conjunction with a +5 V power supply.

The VT2332/3 operates totally asynchronously. No clock input is required. The two programmable Chip Selects allow up to four 32K ROMs to be wired-OR without external decoding. Both devices offer 3-state output buffers for memory expansion.

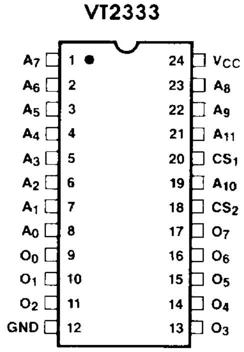
Designed to replace either the 2732 or 2532 32K EPROMs, the VT2332/3 can eliminate the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

PIN CONFIGURATIONS

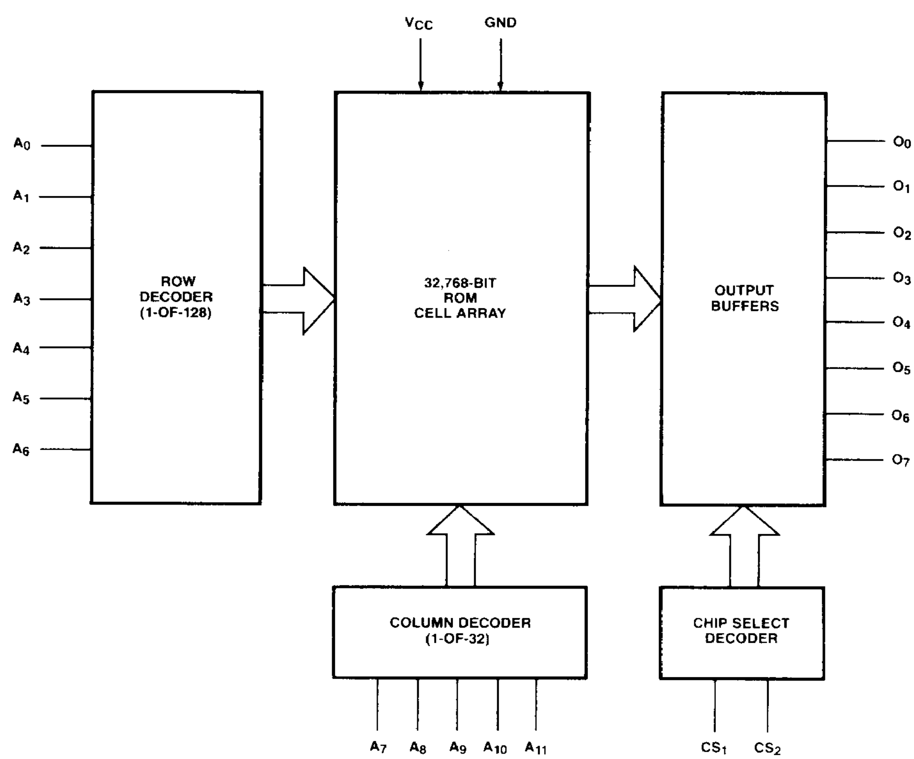
VT2332



VT2333



BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	−10 to +80°C
Storage Temperature	−65 to +150°C
Supply Voltage to Ground Potential	−0.5 to +7.0 V
Applied Output Voltage	−0.5 to +7.0 V
Applied Input Voltage	−0.5 to +7.0 V
Power Dissipation	1.0 W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: T_A = 0 to +70°C, V_{CC} = 5 V ±10% (unless otherwise specified)

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{OH}	Output HIGH Voltage	2.4	V_{CC}	V	V_{CC} = 4.5 V, I_{OH} = −200 μA
V_{OL}	Output LOW Voltage		0.4	V	V_{CC} = 4.5 V, I_{OL} = 2.1 mA
V_{IH}	Input HIGH Voltage	2.0	V_{CC}	V	
V_{IL}	Input LOW Voltage	−0.5	0.8	V	See Note 1
I_{LI}	Input Load Current		10	μA	V_{CC} = 5.5 V, 0 V ≤ V_{IN} ≤ 5.5 V
I_{LO}	Output Leakage Current		10	μA	V_{OUT} = +0.4 V to V_{CC}, Note 2
I_{CC}	Power Supply Current		100	mA	V_{CC} = 5.5 V, V_{IN} = V_{CC}, Note 3

CAPACITANCE: t_A = 25°C, f = 1.0 MHz, Note 4

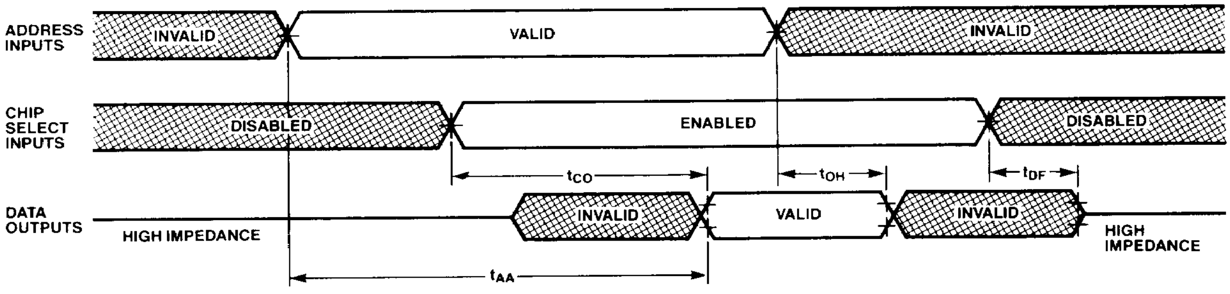
Symbol	Parameter	Min	Max	Unit	Test Conditions
C_I	Input Capacitance		7	pF	All pins except pin under test tied to AC ground
C_O	Output Capacitance		10	pF	

AC CHARACTERISTICS: T_A = 0 to +70°C, V_{CC} = 5 V ±10% (unless otherwise specified)

Symbol	Parameter	VT2332/33		VT2332A/33A		Unit	Test Conditions
		Min	Max	Min	Max		
t_{AA}	Address Access Time		450		300	ns	Output load: 1 TTL load and 100 pF Input transition time: 20 ns Timing reference levels: Input: 1.5 V Output: 0.8 V and 2.0 V
t_{CO}	Chip Select Delay		150		100	ns	
t_{DF}	Chip Deselect Delay		150		100	ns	
t_{OH}	Output Hold After Address Change	20		20		ns	

Notes:
1. Input levels that swing more negative than −0.5 V will be clamped and may cause damage to the device.
2. Measured with device deselected.
3. Measured with device selected and outputs unloaded.
4. This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAM



PROGRAMMING INSTRUCTIONS

All VTI Read Only Memories utilize computer-aided techniques to manufacture and test custom bit patterns. The custom bit pattern and address information is supplied on standard 80-column computer cards or 1" wide paper tape.

CARD FORMAT

All addresses and related output patterns must be completely defined. Each deck of cards defining a specific ROM bit pattern consists of 1) four Title Cards and 2) address and bit pattern Data Cards. Positive logic is generally used on all input cards: a logic "1" is the most positive or HIGH level, and a logic "0" is the most negative or LOW level. VTI can also accept ROM data in other formats, compatible with most microprocessors and PROMs. Consult your VTI representative for details.

TITLE CARDS

A set of four Title Cards should accompany each data deck. These cards give our computer programs additional information necessary to accurately produce high-density ROMs. These four Title Cards must contain the following information:

COLUMN	INFORMATION
FIRST CARD	
1–30	Customer name
31–50	Customer part number
60–72	VTI part number (punch VT2332 or VT2333)
SECOND CARD	
1–30	Customer contact (name)
31–50	Customer Telephone number
THIRD CARD	
1–6	Leave blank—pattern number to be assigned by VTI
30	CS2/$\overline{CS_2}$ Chip Select logic level (if LOW selects chip, punch "0"; if HIGH selects chip, punch "1"; if DON'T CARE, punch "2"
31	CS1/$\overline{CS_1}$ Chip Select logic level.
FOURTH CARD	
1–8	Data Format Punch "Intel" starting in column one.
15–28	Logic Format; punch "POSITIVE LOGIC" or "NEGATIVE LOGIC."
35–37	Truth table verification code; punch either "VERIFICATION HOLD" (manufacturing starts after customer approval of bit pattern data supplied by VTI) or "VERIFICATION NOT NEEDED" (manufacturing starts immediately upon receipt of customer card deck).

INTEL DATA CARD FORMAT

Output data is punched as either a "P" or an "N"; a "P" is defined as a HIGH and an "N" is defined as a LOW. Output 8 (O_8 or O_7) is the MSB and Output 1 (O_1 or O_0) is the LSB. The four Title Cards listed above must accompany the Intel card deck.

COLUMN	INFORMATION
DATA CARDS	
1–5	Punch the 5-digit decimal equivalent of the binary coded address which begins each card. This is the initial input address. The address is right justified, i.e. 00000, 00008, 00016, etc.
7–14	Output data (MSB-LSB) for initial input address.
16–23	Output data for initial input address + 1
25–32	Output data for initial input address + 2
34–41	Output data for initial input address + 3
43–50	Output data for initial input address + 4
52–59	Output data for initial input address + 5
61–68	Output data for initial input address + 6
70-77	Output data for initial input address + 7
79–80	ROM pattern number (may be left blank)

INTEL PAPER TAPE FORMAT

The paper tape which should be used is 1" wide paper tape using 7 or 8-bit ASCII code, such as a model 33 ASR teletype produces.

BPNF FORMAT

The format requirements are as follows:

1. All word fields are to be punched in consecutive order, starting with word field 0 (all addresses LOW). There must be exactly N word fields for the N x 8 ROM organization.
2. Each word field must begin with the start character B and end with the stop character F. There must be exactly eight data characters between the B and F for the N x 8 organization.
   NO OTHER CHARACTERS, SUCH AS RUBOUTS, ARE ALLOWED ANYWHERE IN A WORD FIELD. If in preparing a tape, an error is made, the entire word field, including the B and F must be rubbed out. Within the word field, a P results in a HIGH tape level output, and an N results in a LOW level output.
3. Preceding the first word field and following the last word field, there must be a leader/trailer length of at least 25 characters. This should consist of rubout punches (letter key for Telex tapes).
4. Between word fields, comments not containing B's or F's may be inserted. Carriage return and line feed characters should be inserted (as a "comment") just before each word field (or at least between every 4-word fields). When these carriage returns, etc. are inserted, the tape may be easily listed on the teletype for purposes of error checking. The customer may also find it helpful to insert the word number (as a comment) at least every 4-word fields.
5. Included in the tape before the leader should be the customer's complete Telex or TWX number and if more than one pattern is being transmitted, the ROM pattern number.
6. MSB and LSB are the most and least-significant bit of the device outputs. Refer to the data sheet for the pin numbers.

HEXADECIMAL PROGRAM TAPE FORMAT

The hexadecimal tape format used by the INTELLEC 8 system is a modified memory image, blocked into discrete records. Each record contains record length, record type, memory address, and checksum information in addition to data. A frame by frame description is as follows:

FRAME 0
Record mark. Signals the start of a record. The ASCII character colon (":" HEX 3A) is used as the record mark.

FRAMES 1,2 (0-9, A-F)
Record length. Two ASCII characters representing a hexadecimal number in the range 0 to 'FF' (0 to 255). This is the count of the actual data bytes in the record type or checksum. A record length of 0 indicates end of file.

FRAMES 3 TO 6
Load Address. Four ASCII characters that represent the initial memory will be loaded. The first data byte is stored in the location pointed to by the load address, succeeding data bytes are loaded into ascending addresses.

FRAMES 7,8
Record type. Two ASCII characters. Currently all records are type 0, this field is reserved for future expansion.

FRAMES 9 to 9+2* (RECORD LENGTH) −1
Data. Each 8-bit memory word is represented by two frames containing the ASCII characters (0 to 9, A to F) to represent a hexadecimal value 0 to 'FF' (0 to 255).

HEXADECIMAL PROGRAM TAPE FORMAT (cont.)

FRAMES 9+2* (RECORD LENGTH) TO 9+2* (RECORD LENGTH) +1
Checksum. The checksum is the negative of the sum of all 8-bit bytes in the record since the record mark (":") evaluated modulus 256. That is, if you add together all the 8-bit bytes, ignoring all carries out of an 8-bit sum, then add the checksum, the result is zero.

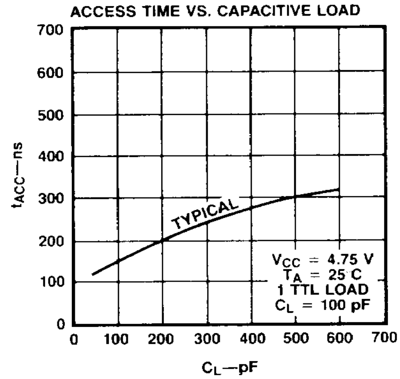
Example: If memory locations 1 through 3 contain 53F8EC, the format of the hex file produced when these locations are punched is:

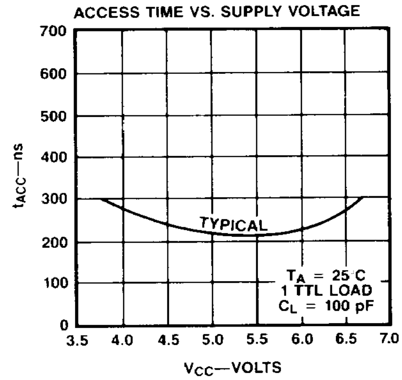
:0300010053F8ECC5

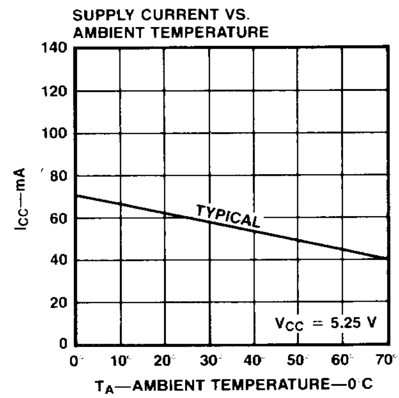
Send bit pattern data to the following address:

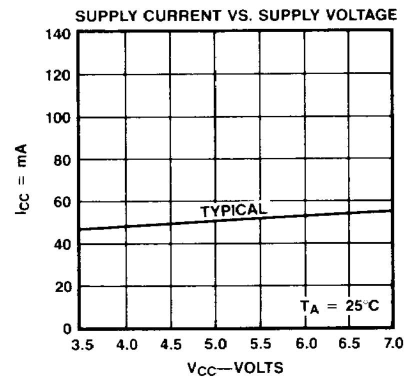
VTI-ROM
1101 McKay Drive
San Jose, CA 95131

TYPICAL CHARACTERISTICS



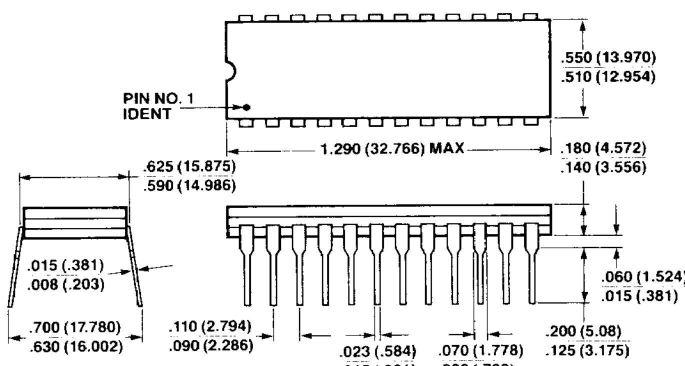






PACKAGE DIAGRAMS

24-LEAD CERDIP DUAL IN-LINE



24-LEAD PLASTIC DUAL IN-LINE